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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,924	08/31/2000	Michael S Bertone	1662-31400 (P00-3212)	4257

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EXAMINER	
NGUYEN, DUSTIN	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,924	BERTONE ET AL.	
	Examiner	Art Unit	
	Dustin Nguyen	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1 – 20 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Forin [US Patent No 6,594,701].

4. As per claim 14, Forin discloses the invention substantially as claimed including a method of allocating space in a shared buffer, comprising:

assigning credits to each source that sends data packets to the shared buffer [col 3, lines 12-15; and lines 40-43]; and

requiring each source to spend a credit each time that source sends a data packet to the shared buffer [col 5, lines 52-55; col 18, lines 45-47 and col 19, lines 18-25];

wherein if the number of empty buffer spaces is larger than a buffer threshold, immediately paying the credit back to the source from which the credit and data were sent [col 5, lines 47-67; and col 20, lines 50-65]; and

wherein if the number of empty buffer spaces is smaller than the buffer threshold, holding the credit until a buffer space becomes empty and then paying a credit back to a source from which a credit was sent [col 18, lines 61-col 19, lines 18; and col 20, lines 37-49].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 7-12 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forin [US Patent No 6,594,701], in view of Hagersten et al. [US Patent No 5,958,019].

7. As per claim 1, Forin discloses the invention substantially as claimed including a multi-processor computer system, comprising:

memory controller allocates the memory requests in a shared buffer using a credit-based allocation scheme [Abstract; and col 3, lines 36-39].

Forin does not specifically disclose

a plurality of processors, each processor coupled to at least one memory cache, one cache control unit, and one interprocessor router;

a memory coupled to each processor, each memory managed by a memory controller configured to accept memory requests from the plurality of processors; and

at least one input/output device coupled to at least one processor;

wherein the memory requests from a local processor are delivered to the memory controller by the cache control unit and wherein memory requests from other processors are delivered to the memory controller by the interprocessor router.

Hagersten discloses

a plurality of processors, each processor coupled to at least one memory cache, one cache control unit, and one interprocessor router [32A-D, 34A-D, 38, Figure 1A; and col 9, lines 19-24];

a memory coupled to each processor, each memory managed by a memory controller configured to accept memory requests from the plurality of processors [36A-D, Figure 1A]; and

at least one input/output device coupled to at least one processor [26, Figure 1];

wherein the memory requests from a local processor are delivered to the memory controller by the cache control unit and wherein memory requests from other processors are delivered to the memory controller by the interprocessor router [col 8, lines 3-21].

It would have been to a person skill in the art at the time the invention was made to combine the teaching of Forin and Hagersten because Hagersten's teaching would allow to speed up the processing of information to increase system performance.

8. As per claim 2, Forin discloses wherein:

the cache control unit and the interprocessor router are each assigned a number of credits [col 3, lines 12-15; and lines 40-43];

at least one of said credits must be delivered by the cache control unit to the memory controller when a memory request is delivered by the cache control unit to the memory controller [74, 97, Figure 3; and col 5, lines 5-16]; and

at least one of said credits must be delivered by the interprocessor router to the memory controller when a memory request is delivered by the interprocessor router to the memory controller [97, Figure 3; and col 6, lines 1-5]:

wherein if the number of filled spaces in the shared buffer is below a threshold, the buffer return the credits to the source from which the credit and memory request arrived [col 5, lines 47-67; and col 20, lines 50-65].

9. As per claim 3, Forin discloses wherein:

wherein if the number of filled spaces in the shared buffer is above a threshold, the buffer holds the credits and returns a credit in a round-robin manner to a source from which a credit has been received only when a space in the shared buffer becomes free [col 18, lines 61-col 19, lines 18; and col 20, lines 37-49]; and

wherein if a source has no available credits, that source cannot deliver a memory request to the shared buffer [col 3, lines 28-31].

10. As per claim 4, Forin discloses wherein:

the number of credits assigned to the cache control unit and the interprocessor router is sufficient to enable each source to deliver an uninterrupted burst of memory requests to the buffer without having to wait for credits to return from the buffer [col 19, lines 56-col 20, lines 14].

11. As per claim 5, Forin discloses wherein:

the number of credits available in the cache control unit and the interprocessor router are stored and updated in counters located in the cache control unit and the interprocessor router [col 15, lines 1-9]; and

the number of credits spent by the cache control unit and the interprocessor router are stored and updated in counters located in the shared buffer [col 19, lines 35-40].

12. As per claim 7, it is rejected for similar reasons as stated above in claims 1 and 14. Furthermore, Forin discloses a front-end directory in-flight table [Abstract]. Forin does not specifically disclose L2 data cache and L2 instruction and data cache control unit configured to send request and response commands from the processor to the memory controller. Hagersten discloses L2 data cache [18A, 18B, Figure 1] and L2 instruction and data cache control unit configured to send request and response commands from the processor to the memory controller [52, 54, Figure 2]. It would have been obvious to a person skill the art at the time the invention was made to combine the teaching of Forin and Hagersten because Hagersten's teaching of L2 cache would provide additional level of caching to increase system performance.

13. As per claim 8, Forin discloses wherein:

if the request buffer is filled above a buffer threshold, the directory in-flight table holds credits and returns a credit to a source from which a credit was received only when a buffer space is emptied [col 15, lines 8-10]; and

wherein if a source has no available credits, that source may not send a request or response command to the request buffer and wherein if a source has one available credits, that source may only send a response command to the request buffer [col 3, lines 26-34].

14. As per claim 9, Forin discloses wherein:

the credits are returned to the sources which have given up credits to the directory in-flight 3 table in a random, equally probably manner [col 5, lines 47-56].

15. As per claim 10, it is rejected for similar reasons as stated above in claims 6 and 7.

16. As per claims 11 and 12, they are rejected for similar reasons as stated above in claims 5 and 14.

17. As per claim 15, it is rejected for similar reasons as stated above in claim 9.

18. As per claim 16, Forin discloses wherein:

when the number of empty buffer spaces is smaller than the buffer threshold and a buffer

space becomes empty, returning a credit in a random, statistically skewed manner to one of the sources which have spent credits held by the buffer [col 19, lines 45-56].

19. As per claim 17, Forin discloses

assigning a minimum number of credits to each source that is sufficient to allow each source to send a continuous sequence of data packets without waiting for returned credits [col 19, lines 37-39].

20. As per claim 18, it is rejected for similar reasons as stated above in claim 3.

21. As per claim 19, Forin discloses setting the buffer threshold equal to the number of total credits assigned to all the sources [col 6, lines 44-46].

22. As per claim 20, it is rejected for similar reasons as stated above in claim 5.

23. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forin [US Patent No 6,594,701], in view of Hagersten et al. [US Patent No 5,958,019], and further in view of Shah et al. [US Patent No 6,347,337].

24. As per claim 6, Forin and Hagersten do not specifically disclose wherein:

the threshold is the point when the number of free spaces available in the buffer is equal to the total number of credits assigned to the cache control unit and the interprocessor router.

Shah discloses

the threshold is the point when the number of free spaces available in the buffer is equal to the total number of credits assigned to the cache control unit and the interprocessor router [col 13, lines 41-50].

It would have been obvious to a person skill the art at the time the invention was made to combine the teaching of Forin, Hagersten and Shah because Shah's teaching would allow to manage buffer size to provide continuous flow of information.

25. As per claim 13, it is rejected for similar reasons as stated above in claim 4. Furthermore, Forin and Hagersten do not specifically disclose wherein the number of credits available to the L2 instruction and data cache control unit and interprocessor and 110 router is determined by the round trip time required to send a credit to and receive a credit from the directory in-flight table. Shah discloses the number of credits available to the L2 instruction and data cache control unit and interprocessor and 110 router is determined by the round trip time required to send a credit to and receive a credit from the directory in-flight table [Figure 6; and col 9, lines 24-41]. It would have been obvious to a person skill the art at the time the invention was made to combine the teaching of Forin, Hagersten and Shah because Shah's teaching of the round trip time would allow the system to have a better determination on delivery of credit according to network bandwidth.

26. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 U.S.C 133, M.P.E.P 710.02, 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (703) 305-5321. The examiner can normally be reached on Monday – Friday (8:00 – 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703) 305-9678.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directly to the receptionist whose telephone number is (703) 305-3900.

Dustin Nguyen

ZARNI MAUNG
PRIMARY EXAMINER